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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,624	06/15/2001	Ian Wylie	WYLIE 5	8470

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EXAMINER

KIELIN, ERIK J

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 02/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/882,624

Applicant(s)

WYLIE, IAN

Examiner

Erik Kielin

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-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 June 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 June 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested:

A transistor with source and drain regions formed above the isolation region and method of manufacture.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the additional active and passive devices as required in claim 33, the isolation region formed *adjacent* the semiconductor substrate as required in claims 2 and 28 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

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4. Claims 2 and 28 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is not possible to form an isolation region "adjacent" a semiconductor substrate. The term "adjacent" means nearby or next to or having a common endpoint. (See any dictionary.) There is no basis in the art for forming an isolation region which is only adjacent to the semiconductor substrate, as it would be without use. Instead it is known in the art to form isolation regions only within the semiconductor substrate to provide electrical isolation between active device regions.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 22 recites the limitation "the semiconductor region" in line 3. There is insufficient antecedent basis for this limitation in the claim.

The claim will be interpreted as best understood by Examiner.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-

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(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

8. Claims 1-4, 7-9, 12, 13, 16, 17, 18, 21-24 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by **Jang** US 5,391,907.

Jang discloses the semiconductor substrate 11, gate 19, source/drain region 20 with a portion formed over the semiconductor substrate and a portion formed on the oxide isolation 18 located in a trench. The channel is formed over the substrate. (See Figs. 2d-2e; col. 2, line 64 to col. 3, line 12.)

Regarding claim 16, Fig. 2e shows the source/drain region of a second transistor at the far right-hand, wherein the isolation region 18 isolates the devices.

9. Claims 1-4, 6, 7-9, 11, 21-24, 26, 27-30, 32 are rejected under 35 U.S.C. 102(e) as being anticipated by **Wong** et al. US 6,246,094 B1.

Wong discloses the semiconductor substrate 2, gates 22, 30, source/drain regions 18, 20, 26, 28 with a portion formed over the semiconductor substrate and a portion formed above the oxide isolation 8,12 located in a trench (called STI and BSTI). The channel is formed over the substrate not over the isolation region. Figure 3B shows that the isolation region extends all the way through the tubs (called wells).

10. Claims 1-4, 7-9, 21-24, 27-30 are rejected under 35 U.S.C. 102(b) as being anticipated by **Yu** et al. US 5,877,046.

Yu discloses the semiconductor substrate 40, gate 57, source/drain regions 50, 52 with a portion formed over the semiconductor substrate and formed on the oxide isolation 46, 48

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located in a trench, and interconnect 62. The channel is formed over the substrate (polysilicon layer 44) not over the isolation region. Plural transistors are disclosed which would be separated by the isolation regions 46, 48.

11. Claims 1-4, 7-9, 12-13, 16, 17-18, 21-24, 27-30, 33 are rejected under 35 U.S.C. 102(b) as being anticipated by **Murakami** US 4,551,743.

Murakami discloses (Fig. 1) the semiconductor substrate 14, gate 21, source/drain regions 19, 20, 52 with a portion formed over the semiconductor substrate and a portion formed on the oxide isolation 11, located in a trench, and interconnect 17, 18, 24, 25. The channel is formed over the substrate, not over the isolation region. Plural transistors are disclosed which would be separated by the isolation regions 11. Other devices are also shown 16-18, 41-43.

12. Claims 1-32 are rejected under 35 U.S.C. 102(b) as being anticipated by **Tsuchiaki** JP 11-274483 A.

Tsuchiaki discloses the semiconductor substrate 11, gates 16a, 19a, source/drain portions 23a, 26a over the oxide isolation regions 12 formed in a trench, which extend through tub ("n-well") 14 and source/drain portions 22, 25 formed in the semiconductor substrate, located in a trench, and interconnect 17, 18, 24, 25. The channel is formed in the substrate, not over the isolation region. Plural transistors are disclosed which are separated by the isolation regions 12. Interconnect 18, 29 is shown in Fig. 5(i) on the last page. (See also Abstract and all figures -- especially the cover figures.)

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Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. Claims 27-30, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Jang** in view of Applicant's admitted prior art (**APA**).

Jang, as explained above, discloses all of the features of the instant invention except for specifically showing the interconnect and other active and passive devices.

Applicant indicates that Fig. 12 shows a conventional integrated circuit (paragraph [0022]) with interconnect 1220 and other active and passive devices and that one of ordinary skill is familiar with these additional elements (paragraph [0044]).

It would have been obvious to one of ordinary skill at the time of the invention to modify **Jang** to include known interconnect and active and passive device in order to form a functioning circuit, such as a DRAM, because it highly desired in the art to form whole integrated circuits rather than just parts which would, in isolation, be useless.

15. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Wong** in view of Applicant's admitted prior art (**APA**).

Wong, as explained above, discloses all of the features of the instant invention except for specifically showing the interconnect and other active and passive devices.

Applicant's APA is applied as above.

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16. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsuchiaki** in view of Applicant's admitted prior art (**APA**).

Tsuchiaki as explained above, discloses all of the features of the instant invention except for specifically showing the interconnect and other active and passive devices.

Applicant's APA is applied as above.


Conclusion

Any inquiry concerning this communication from examiner should be directed to Erik Kielin whose telephone number is (703) 306-5980 and e-mail address is erik.kielin@uspto.gov. The examiner can normally be reached by telephone on Monday through Thursday 9:00 AM until 7:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached at (703) 306-2794 or by e-mail at olik.chaudhuri@uspto.gov. The fax phone number for the group is (703) 308-7722 or -7724.


EK

January 22, 2002


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